

Appendix III

STEBus Module SWI's (parameters normal, results italic)

	SWI	R0	R1	R2	R3	R4	R5	R6
STEBus_rdARCsts	&420C0	slot		<i>data</i>				
STEBus_wrARClat	&420C1	slot		<i>data</i>				
STEBus_rdSTEsts	&420C2	slot		<i>data</i>				
STEBus_wrSTElat	&420C3	slot		<i>data</i>				
STEBus_enableIRQ	&420C4	slot						
STEBus_disableIRQ	&420C5	slot						
STEBus_enableFIQ	&420C6	slot						
STEBus_disableFIQ	&420C7	slot						
STEBus_enableATNinterrupts	&420C8	slot						
STEBus_disableATNinterrupts	&420C9	slot						
STEBus_enableSYSRSTandCYCERRinterrupts	&420CA	slot						
STEBus_disableSYSRSTandCYCERRinterrupts	&420CB	slot						
STEBus_setSYSRST	&420CC	slot						
STEBus_clearSYSRST	&420CD	slot						
STEBus_selectMEM	&420CE	slot						
STEBus_selectIO	&420CF	slot						
STEBus_lock	&420D0	slot						
STEBus_unlock	&420D1	slot						
STEBus_reset	&420D2	slot						
STEBus_STEclri	&420D3	slot						
STEBus_rdATN	&420D4	slot		<i>data</i>				
STEBus_wrADR	&420D5	slot		<i>data</i>				
STEBus_rdIO	&420D6	slot	STEadr	<i>data</i>				
STEBus_wrIO	&420D7	slot	STEadr	<i>data</i>				
STEBus_rdMEM	&420D8	slot	STEadr	<i>data</i>				
STEBus_wrMEM	&420D8	slot	STEadr	<i>data</i>				
STEBus_rdMEMblk	&420DA	slot	STEadr	compadr	count			
STEBus_wrMEMblk	&420DB	slot	STEadr	compadr	count			
STEBus_claimIRQvector	&420DC	slot	intsrc	rtadr	R12			
STEBus_releaseIRQvector	&420DD	slot	intsrc	rtadr	R12			
STEBus_claimFIQ	&420DE	slot	intsrc	rtadr	R10	R11	R12	R13
STEBus_releaseFIQ	&420DF	slot						
STEBus_adrhw	&420E0	slot						

Results (R1 MEMCadr, R2 STEstslatadr, R3 STEstslatadr, R4 STEclriadr, R5 ATNadr ADRadr)

	SWI	R0	R1	R2	R3	R4	R5	R6
STEBus_adrmemADR				&420E1	slot	<i>memADRadr</i>		
STEBus_checkpresent				&420E2	slot			
					<i>status</i>			
STEBus_rdmowrIO				&420E3	slot	STEadr	EORmsk	ANDmsk
STEBus_rdmowrMEM				&420E4	slot	STEadr	EORmsk	ANDmsk

Notes

slot expansion card slot number

data refer to the description in the appropriate part of section 3

STEadr STE memory or IO address

compadr computer's memory address

count number of bytes to read or write

intsrc interrupt source

rtadr address of interrupt handler

R10,R11,R12,R13 values to be passed in Regs R10-R13

MEMCadr base address in the computer's memory of the STEbus I/O or memory space

ARCstslatadr address of status register (read) and control latch (write) on the computer expansion card

STEstslatadr address of status register (read) and control latch (write) on the STEbus board

STEclriadr address of location which when written to clears CYCERR and SYSRST interrupts

ATNadr address of Attention Request status register on the STEbus board

ADRadr address of Address latch on the STEbus board

memADRadr address of the memory copy of the STEbus memory space page status
>0 expansion card present, 0 expansion card not present

EORmsk EOR mask

ANDmsk AND mask